FT7401

Self-Capacitive Touch Panel Controller

INTRODUCTION

The FT7401 Series ICs are single-chip capacitive touch panel controller IC with a built-in 16 bit enhanced Micro-controller unit (MCU).They adopt the self-capacitance technology, which supports single point and gesture touch or two points. In conjunction with a self-capacitive touch panel, The FT7401 Series ICs implement the user-friendly input function and are widely used in various devices.

FEATURES

- Self-Capacitive Sensing Techniques support single point touch and gesture or two point touch
- Absolute X and Y coordinates or gesture
- 1 point and gestures / 2 points supported
- High immunity to RF and power Interferences
- Auto-calibration: Insensitive to Capacitance and Environmental Variations
- Built-in Enhanced MCU
- FT7401 supports up to 46 channels of sensors /drivers
- Report Rate: Up to 100Hz
- Support Interfaces :I2C
- Support single film material TP and triangle pattern without additional shield
- Internal accuracy ADC and smooth filters
- Support 2.8V to 3.6V Operating Voltage
- Support independent IOVCC
- Built-in LDO for Digital Circuits
- High efficient power management with 3 Operating Modes
  - Active Mode
  - Monitor Mode
  - Hibernation Mode
- Operating Temperature Range: -40℃ to +85℃
- ESD:HBM≥7500V,MM≥500V

TABLE OF CONTENTS

1 OVERVIEW

1.1 Typical Applications

FT7401 accommodate a wide range of applications with a set of buttons up to a 2D touch sensing device, their typical applications are listed below.

- Industrial
- GPS
- Game consoles
- POS (Point of Sales) devices
- Portable MP3 and MP4 media players
- Digital cameras
- MIDs

FT7401 series ICs support up to 5.5 inch Touch Panel; users may find out their target IC from the specs listed in the following table,

Model Name	Panel	Package			Touch Panel Size
	Channel	Type	Pin	Size	
FT7401	46	QFN6*6	56	0.6-P0.35	≤5.5 inch

2 FUNCTIONAL DESCRIPTION

2.1 Architectural Overview

Figure2-1 shows the overall architecture for the FT7401.

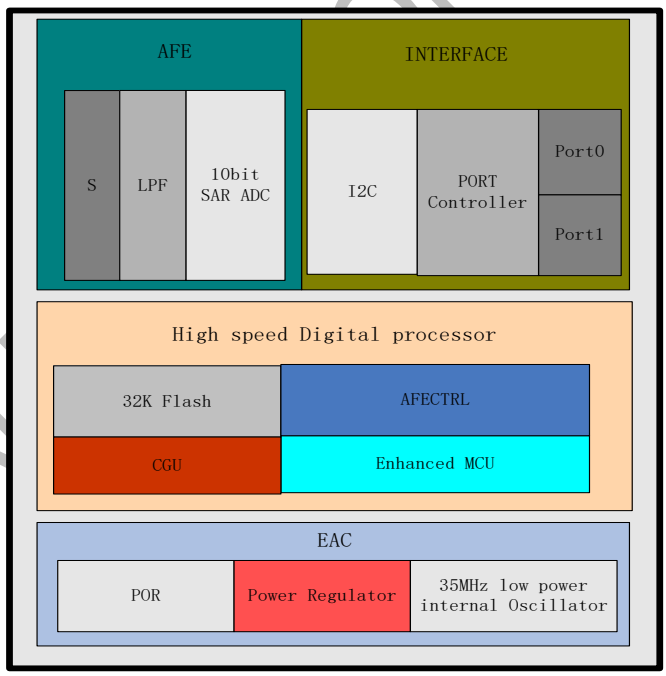


Figure 2-1 FT7401 System Architecture Diagram

The FT7401 is comprised of five main functional parts listed below,

- Touch Panel Interface Circuits

The main function for the AFE and AFE controller is to interface with the touch panel. It scans the panel by sending AC signals to the panel and processes the received signals from the panel. So it supports both driver and Sensor functions. Key parameters to configure this circuit can be sent via serial interfaces.

- Enhanced MCU

For the Enhanced MCU, larger program and data memories are supported. Furthermore, A Flash ROM is implemented to store

programs and some key parameters.
Complex signal Processing algorithms are implemented by MCU to detect the touches reliably and efficiently.
Communication protocol software is also implemented on this MCU to exchange data and control information with the host processor.

- External Interface
  - I2C: an interface for data exchange with host
  - INT: an interrupt signal to inform the host processor that touch data is ready for read
  - RSTN: an external low signal reset the chip.
- A watch dog timer is implemented to ensure the robustness of the chip.
- A voltage regulator to generate 1.8V for digital circuits from the input VDDA supply.

2.2 MCU

This section describes some critical features and operations supported by the Enhanced MCU.

Figure 2-2 shows the overall structure of the MCU block. In addition to the Enhanced MCU core, we have added the following circuits,

- Memory:32KB Flash
- Data Memory: 4KB SRAM
- Timer: A number of timers are available to generate different clocks
- Master Clock:17.5MHz from a 35MHz RC Oscillator
- Clock Manager: To control various clocks under different operation conditions of the system

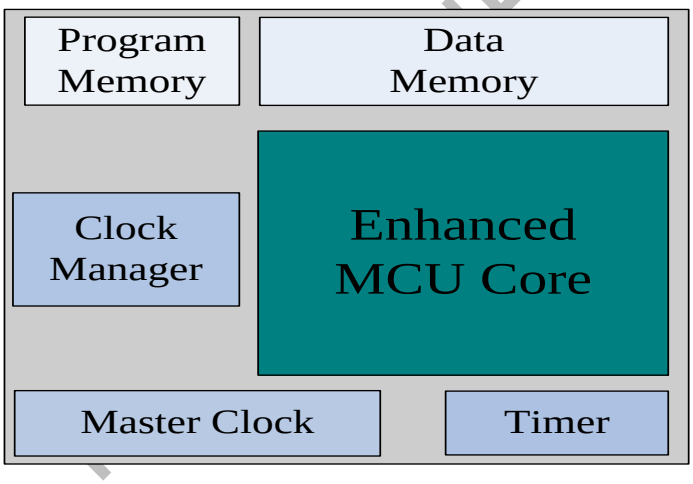


Figure 2-2 MCU Block Diagram

2.3 Operation Modes

FT7401 operates in the following three modes:

- Active Mode

In this mode, FT7401 actively scans the panel. The default scan rate is 60 frames per second. The host processor can configure FT7401 to speed up or to slow down.

- Monitor Mode

In this mode, FT7401 scans the panel at a reduced speed. The default scan rate is 25 frames per second and the host processor can increase or decrease this rate. When in this mode, most algorithms are stopped. A simpler algorithm is being executed to determine if there is a touch or not. When a touch is detected, FT7401 shall enter the Active mode immediately to acquire the touch information quickly. During this mode, the serial port is closed and no data shall be transferred with the host processor

- Hibernation Mode

In this mode, the chip is set in a power down mode. It shall respond to the "RESET" or "Wakeup" signal from the host processor. The chip therefore consumes very little current, which help prolong the standby time for the portable devices.

Host Interface Figure *2-3* shows the interface between a host processor and FT7401. This interface consists of the following three sets of signals:

- Serial Interface

- Interrupt from FT7401 to the Host
- Reset Signal from the Host to FT7401

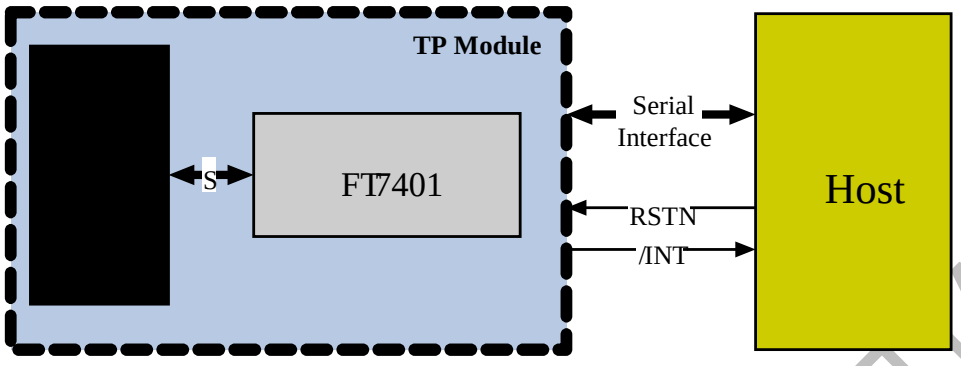


Figure 2-3 Host Interface Diagram

The serial interface of FT7401 is I2C. The details of this interface are described in detail in Section 2.5. The interrupt signal (/INT) is used for FT7401 to inform the host that data are ready for the host to receive. The RSTN signal is used for the host to reset FT7401. After resetting, FT7401 shall enter the Active mode.

2.4 Serial Interface

FT7401 supports the I2C interfaces, which can be used by a host processor or other devices.

2.4.1 I2C

The I2C is always configured in the Slave mode. The data transfer format is shown in Figure 2-4.

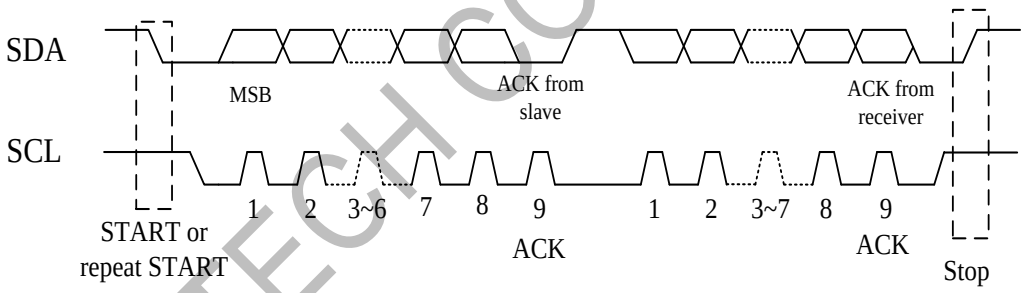


Figure 2-4 I2C Serial Data Transfer Format

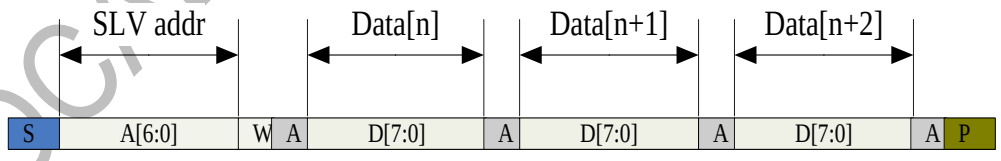


Figure 2-5 I2C master write, slave read

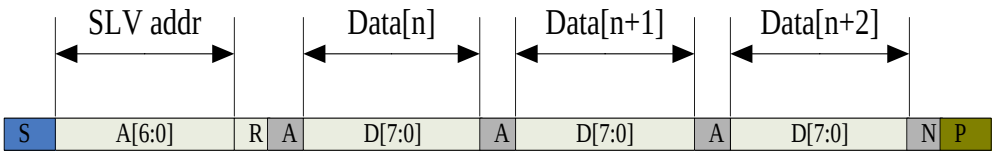


Figure 2-6 I2C master read, slave write

Table 2-1 lists the meanings of the mnemonics used in the above figures.

Table 2-1 Mnemonics Description

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address
R/W	READ/WRITE bit, '1' for read, '0'for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

I2C Interface Timing Characteristics is shown in Table 2-2.

Table 2-2 I2C Timing Characteristics

Parameter	Min	Max	Unit
SCL frequency	10	400	KHz
Bus free time between a STOP and START condition	4.7	\	us
Hold time (repeated) START condition	4.0	\	us
Data setup time	250	\	ns
Setup time for a repeated START condition	4.7	\	us
Setup Time for STOP condition	4.0	\	us

3 ELECTRICAL SPECIFICATIONS

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Power Supply Voltage	VDDA - VSSA	-0.3 ~ +3.6	V	1, 2
Power Supply Voltage2	VDD3 - VSS	-0.3 ~ +3.6	V	1, 3
I/O Digital Voltage	IOVCC	1.8~3.6	V	1
Operating Temperature	Topr	-40 ~ +85	℃	1
Storage Temperature	Tstg	-55 ~ +150	℃	1

Notes

1. If used beyond the absolute maximum ratings, FT7401 may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device. The lower limit voltage can support 5% drop if application needed
2. Make sure VDDA (high) ≥VSSA (low).

3.2 DC Characteristics

Table 3-2 DC Characteristics (VDDA=2.8~3.6V, Ta=-40~85℃)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit	Note
Input high-level voltage	VIH		0.7 x IOVCC	-	IOVCC	V	
Input low -level voltage	VIL		-0.3	-	0.3 x IOVCC	V	
Output high -level voltage	VOH	IOH=-0.1mA	0.7 x IOVCC	-	-	V	
Output low -level voltage	VOL	IOH=0.1mA	-	-	0.3 x IOVCC	V	

I/O leakage current	ILI	Vin=0~VDDA	-1	-	1	μA	
Current consumption （Normal operation mode）	Iopr	VDDA =VDD3= 2.8V Ta=25℃ MCLK=17.5MHz	-	4	-	mA	
Current consumption （Monitor mode）	Imon	VDDA =VDD3= 2.8V Ta=25℃ MCLK=17.5MHz	-	1.5	-	mA	
Current consumption （Sleep mode）	Islp	VDDA =VDD3= 2.8V Ta=25℃ MCLK=17.5MHz	-	50	-	uA	
Step-up output voltage	VDD5	VDDA = VDD3=2.8V	-	5	-	V	
Power Supply voltage	VDDA VDD3		2.8	-	3.3	V	

3.3 AC Characteristics

Table 3-3 AC Characteristics of Oscillators

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
OSC clock 1	fosc1	VDDA= 2.8V；Ta=25℃	34.65	35	35.35	MHz	

Table 3-4 AC Characteristics of sensor

Item	Symbol	Test Condition	Min	Typ.	Max	Unit	Note
Sensor acceptable clock	ftx	VDDA= 2.8V；Ta=25℃	0	100	300	KHz	
Sensor output rise time	Ttxr	VDDA= 2.8V；Ta=25℃	-	100	-	nS	
Sensor output fall time	Ttxf	VDDA= 2.8V；Ta=25℃	-	80	-	nS	
Sensor input voltage	Trxi	VDDA= 2.8V；Ta=25℃	-	5	-	V	

3.4 I/O Ports Circuits

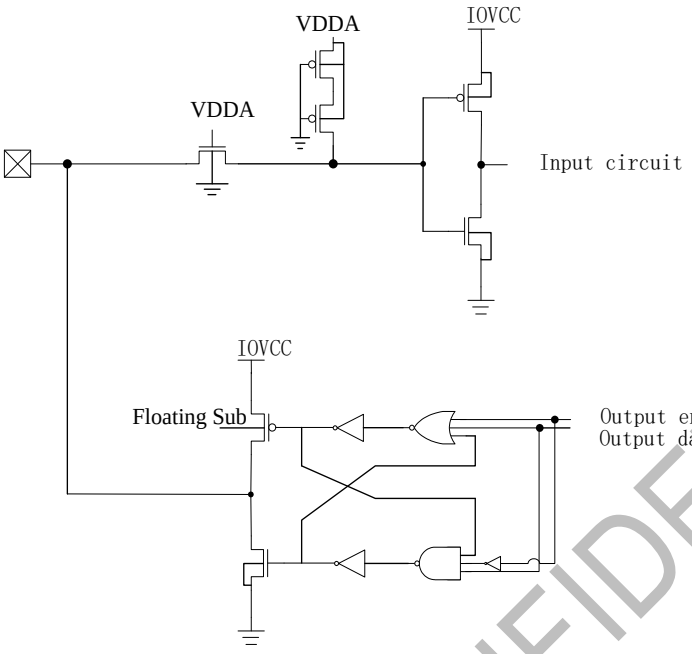


Figure 3-1 Digital In/Out Port Circuit

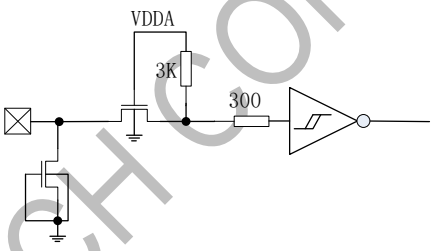


Figure 3-2 Reset Input Port Circuits

3.5 POWER ON/Reset/Wake Sequence

The GPIO such as INT and I2C are advised to be low before powering on. Reset should be pulled down to be low before powering on. INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Trst is more than 5ms.

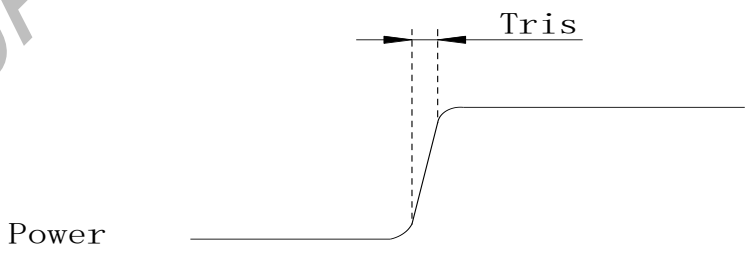


Figure 3-7 Power on time

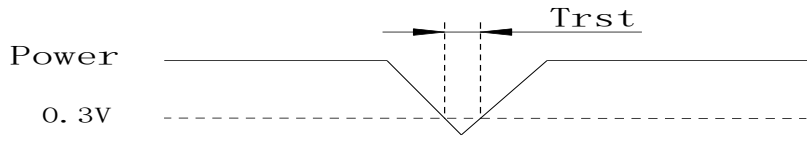


Figure 3-8 Power Cycle requirement

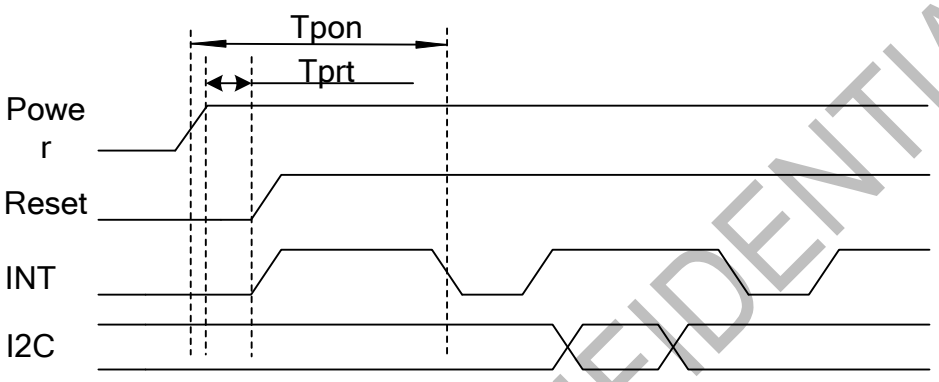


Figure 3-9 Power on Sequence

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

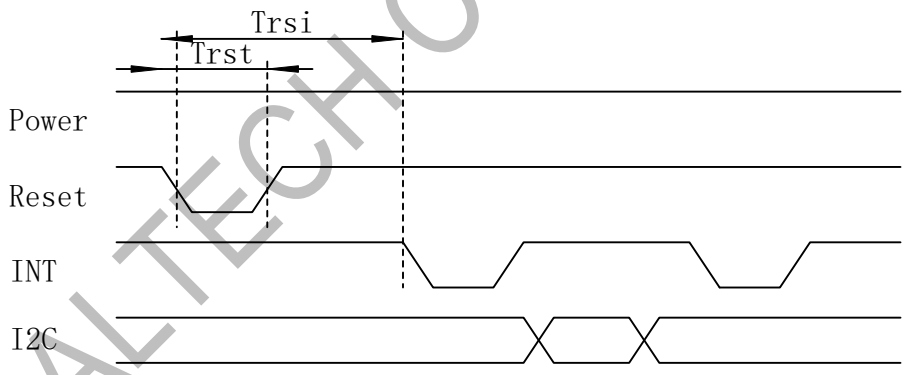


Figure 3-10 Reset Sequence

Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	-	3	ms
Tpon	Time of starting to report point after powering on	300	-	ms
Tprt	Time of being low after powering on	1	-	ms
Trsi	Time of starting to report point after resetting	300	-	ms
Trst	Reset time	5	-	ms

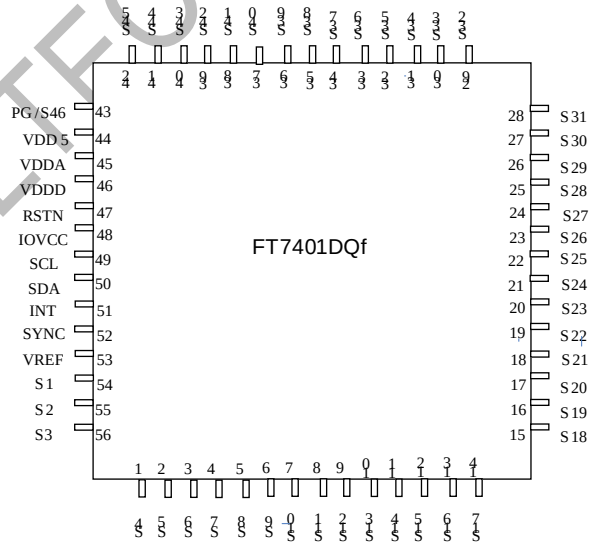
4 PIN CONFIGURATIONS

Pin List of FT7401

Table 4-1 Pin Definition of FT7401

Name	Pin No.	Type	Description
	FT7401 DQf		
VREF	53	PWR	Generated internal reference voltage. A 1μF ceramic capacitor to ground is required.
S1	54	I/O	Capacitance sensor /driver channel
S2	55	I/O	Capacitance sensor /driver channel
S3	56	I/O	Capacitance sensor /driver channel
S4	1	I/O	Capacitance sensor /driver channel
S5	2	I/O	Capacitance sensor /driver channel
S6	3	I/O	Capacitance sensor /driver channel
S7	4	I/O	Capacitance sensor /driver channel
S8	5	I/O	Capacitance sensor /driver channel
S9	6	I/O	Capacitance sensor /driver channel
S10	7	I/O	Capacitance sensor /driver channel
S11	8	I/O	Capacitance sensor /driver channel
S12	9	I/O	Capacitance sensor /driver channel
S13	10	I/O	Capacitance sensor /driver channel
S14	11	I/O	Capacitance sensor /driver channel
S15	12	I/O	Capacitance sensor /driver channel
S16	13	I/O	Capacitance sensor /driver channel
S17	14	I/O	Capacitance sensor /driver channel
S18	15	I/O	Capacitance sensor /driver channel
S19	16	I/O	Capacitance sensor /driver channel
S20	17	I/O	Capacitance sensor /driver channel
S21	18	I/O	Capacitance sensor /driver channel
S22	19	I/O	Capacitance sensor /driver channel
S23	20	I/O	Capacitance sensor /driver channel
S24	21	I/O	Capacitance sensor /driver channel
S25	22	I/O	Capacitance sensor /driver channel
S26	23	I/O	Capacitance sensor /driver channel
S27	24	I/O	Capacitance sensor /driver channel
S28	25	I/O	Capacitance sensor /driver channel
S29	26	I/O	Capacitance sensor /driver channel
S30	27	I/O	Capacitance sensor /driver channel
S31	28	I/O	Capacitance sensor /driver channel
S32	29	I/O	Capacitance sensor /driver channel
S33	30	I/O	Capacitance sensor /driver channel
S34	31	I/O	Capacitance sensor /driver channel
S35	32	I/O	Capacitance sensor /driver channel
S36	33	I/O	Capacitance sensor /driver channel
S37	34	I/O	Capacitance sensor /driver channel

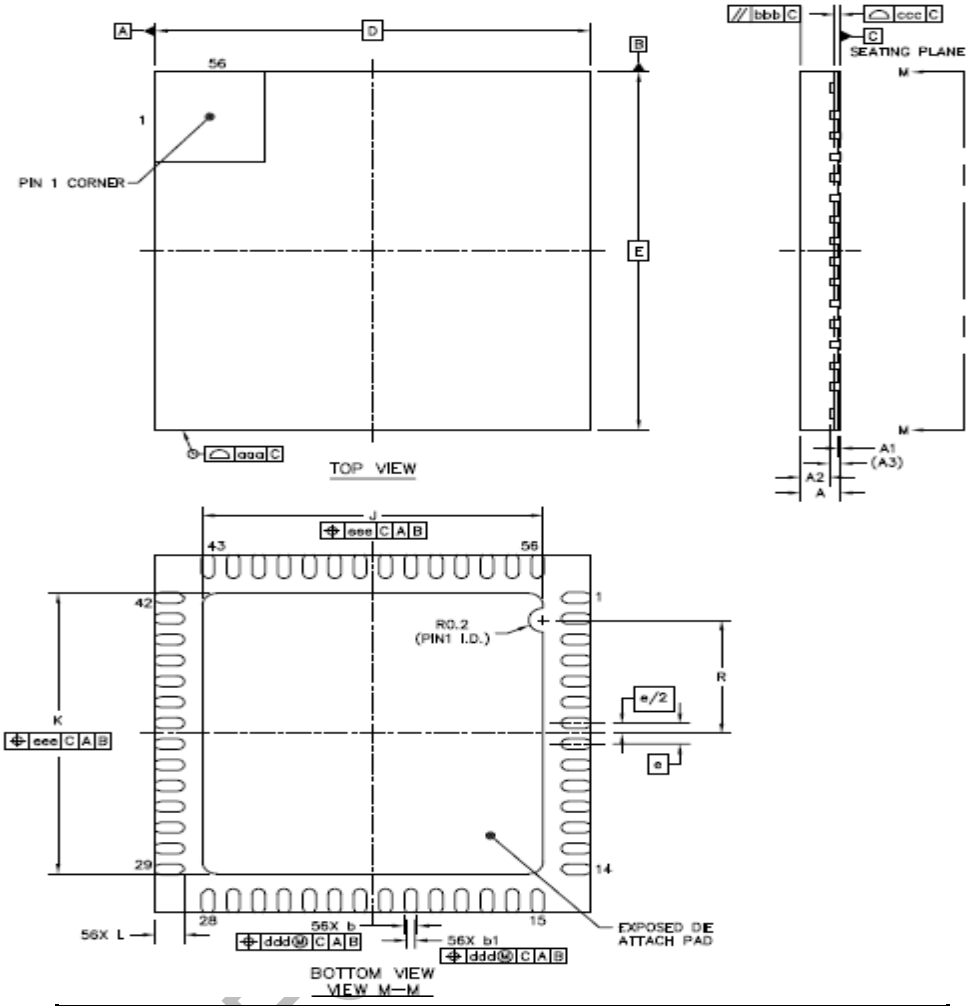
S38	35	I/O	Capacitance sensor /driver channel
S39	36	I/O	Capacitance sensor /driver channel
S40	37	I/O	Capacitance sensor /driver channel
S41	38	I/O	Capacitance sensor /driver channel
S42	39	I/O	Capacitance sensor /driver channel
S43	40	I/O	Capacitance sensor /driver channel
S44	41	I/O	Capacitance sensor /driver channel
S45	42	I/O	Capacitance sensor /driver channel
S46	43	I/O	Capacitance sensor /driver channel
VDD5	44	PWR	High voltage power supply from the charge pump LDO generated internally. A 1μF ceramic to ground is required.
VSSA		GND	Analog ground
VDDA	45	PWR	Analog power supply, A 1μF ceramic capacitor to ground is required.
VSS		GND	Analog ground
VDDD	46	PWR	Digital power supply. A 1μF ceramic capacitor to ground is required.
VSSD		GND	Analog ground
RSTN	47	I	External Reset, Low is active
IOVCC	48	PWR	I/O power supply
SCL	49	I/O	I2C clock input
SDA	50	I/O	I2C data input and output
INT	51	I/O	External interrupt to the host
SYNC	52	I/O	NC



FT7401DMf Package Diagram

5 PACKAGE INFORMATION

5.1 Package Information of QFN-6x6-56L Package



Item	Symbol	Millimeter		
		Min	Type	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	----	0.4	----
L/F Thickness	A3		0.152 REF	
Lead Width	b	0.13	0.18	0.23
	b1	0.07	0.12	0.17
Body Size	D		6 BSC	
	E		6 BSC	
Lead Pitch	e		0.35 BSC	
EP Size	J	4.6	4.7	4.8
	K	4.6	4.7	4.8
Lead Length	L	0.35	0.4	0.45
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.1	
Co Planarity	ccc		0.08	
Lead Offset	ddd		0.1	
Exposed Pad Offset	eee		0.1	

5.2 Order Information

Package Type	QFN
	56Pin(6*6)
	0.6-P0.35
Product Name	FT7401DQf

Note:

1). The last two letters in the product name indicate the package type and thickness and lead pitch.

2). The three last letter indicates the package type..

D : QFN-6*6

3). The second last letter indicates the thickness and lead pitch.

Q : 0.6-P0.35

4). The last letter indicates the numbers of sensors.

f： 46

T: Track Code

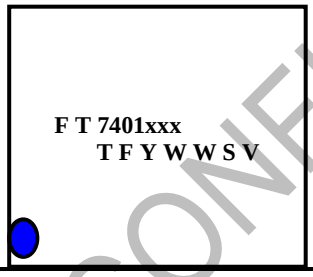
F/R:"F" for Lead Free process,

"R" for Halogen Free process

Y: Year Code

WW: Week Code

S: Lot Code



V：IC Version

Product Name	Package Type	Pannel Channels
FT7401DQf	**QFN-56L(6*6)**	**46**

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